



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/603,281	06/24/2003	Rong Yin	02-C-084	4449
7590 08/27/2004				
Lisa K. Jorgenson, Esq. STMicroelectronics, Inc. 1310 Electronics Drive Carrollton, TX 75006-5039		EXAMINER CHANG, JOSEPH		
		ART UNIT PAPER NUMBER		
		2817		

DATE MAILED: 08/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/603,281

Applicant(s)

YIN, RONG

Examiner

Joseph Chang

Art Unit

2817

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-25 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,4,12,16,17 and 19-22 is/are rejected.
- 7) ☒ Claim(s) 2,3,5-11,13-15,18 and 23-25 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 24 June 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_.
- ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_.
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: \_\_\_\_.

## **DETAILED ACTION**

### ***Specification***

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: CONTROL CIRCUIT AND METHOD FOR CRYSTAL OSCILLATOR USING A TIMER.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 4, 12, 16 and 17 are rejected under 35 U.S.C. 102(e) as being anticipated by Mar (US 6563391).

Regarding Claim 1, Mar discloses in figures 1-6, an oscillator circuit (10), comprising: a crystal oscillator circuit (Crystal 20, Amplifier Module 30) adapted to oscillate at approximately a predetermined frequency (intrinsic characteristic of the crystal); and a control circuit (Control Module 40) coupled to the crystal oscillator circuit (via Bias Module 60) for controlling a current level (Col. 3, lines 66-67, Col. 4, lines 36-38) at which the crystal oscillator circuit operates (oscillation), the control circuit (40) selectively switching the current level from a first current level (2.0 microamps) to a

Art Unit: 2817

second current level (2.5 microamps) (Col. 5, lines 13-20) different from the first current level a predetermined period of time (form of a finite pulse) following an occurrence of an event (START)(Col. 5, lines 35-43).

Regarding Claim 4, Figure 4 shows at least two flip-flop circuits (403, 404), at least one of the at least two flip-flop circuits adapted to receive a clock signal (CK).

Regarding Claim 12, Mar discloses a method (an oscillator circuit (10) would necessarily perform the method claimed) for generating an oscillating signal, comprising: generating, at a first current level (2.0 microamps) (Col. 5, lines 13-20), an output signal (output at node 94, CLK32K) to oscillate between at least two voltage levels at around a predetermined frequency (clock frequency), each voltage level corresponding to a distinct logic state (clock level)(intrinsic property of the output clock); receiving an input signal (START) having a value (a several nanoseconds) indicative an occurrence of an event (startup); and after at least a predetermined period time (a several nanoseconds) following the input signal (START) having the value (a several nanoseconds) indicative of the occurrence of the event (startup), generating, at a second current level (2.5 microamps) (Col. 5, lines 13-20) different from the first current level (2.0), the output signal to oscillate at around the predetermined frequency (intrinsic functionality of the oscillator output).

Regarding Claim 16, Mar discloses a first, second, third and fourth startup values as 2.0, 2.5, 3.0 and 3.5 in microamps respectively. The startup values are selectable based on the input control signal. Thus, when the forth startup value is selected at the

Art Unit: 2817

startup, it becomes a first current level and one of the others becomes a second current level, and hence the second current level is less than the first current level.

Regarding Claim 17, Mar discloses that the event (startup) is completion of a power-up sequence (Col.5. lines 35-44).

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 19-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mar in view of Hongo (5923838).

Regarding Claims 19, Mar discloses an oscillator circuitry (90) in Figures 1-6 adapted to generate a signal (CLK32K, output of 94) at a first current (2.0 microamps) and, subsequent to approximately a predetermined period of time (a several nanoseconds) after an occurrence of an event (startup, (Col.5. lines 35-44)), at a second current level (2.5 microamps) different from the first current level (2.0 microamps). Further discloses that the oscillator circuitry provides low power consumption. However, Mar does not explicitly disclose its application - a system comprising a circuitry responsive to at least one signal that oscillates at approximately a predetermined frequency.

As would have been well known in the art, an oscillator has been used in a microcomputer system for providing a clock that is required to run the system. (Hongo reference is only to show a typical microcomputer configuration having a processor that is a circuitry responsive to a clock that oscillates at approximately a predetermined frequency). As stated above, Mar provides an oscillator that has low power consumption.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the invention to apply an oscillator circuitry of Mar in a microcomputer system for its use as a source of clock because such application would have advantageously provided the low power consumption.

Regarding Claim 20, Mar discloses a first, second, third and fourth startup values as 2.0, 2.5, 3.0 and 3.5 in microamps respectively. The startup values are selectable based on the input control signal. Thus, when the forth startup value is selected at the startup, it becomes a first current level and one of the others becomes a second current level, and hence the second current level is less than the first current level

Regarding Claim 21, a power-up sequence in described in Col.5. lines 35-44.

Regarding Claim 22, powering up from a battery would be obvious to one of ordinary skill in the art at the time of the invention because it would have provided the benefit of portability. (It is noted that Mar implies that his oscillator circuitry is powered by a battery because battery requires low power consumption in order to prolong its life, which Mar provides an oscillator circuitry that has low power consumption).

***Allowable Subject Matter***

Claims 2, 3, 5-11, 13-15, 18 and 23-25 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: the best prior art of record, Shinmori, taken alone or in combination of other references, does not teach or fairly suggest a timer (Claims 2, 3, 5-11, 13-15, 23-25), or a method in Claim 18.

***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Sibrai et al. discloses a crystal oscillator using AGC to reduce power consumption.

Mourant et al. discloses a crystal oscillator using a current mirror to improve long-term frequency stability.

Aihara et al. discloses a crystal oscillator using CMOSFET to reduce power consumption.

Senthilkumar et al. discloses a crystal oscillator using a constant current bias to reduce power consumption.

Art Unit: 2817

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Chang whose telephone number is 571 272-1759. The examiner can normally be reached on Mon-Fri 0700-1730.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on (571) 272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A handwritten signature in black ink, reading "Joseph Chang". The signature is written in a cursive, flowing style.

Joseph Chang  
Patent Examiner  
Art Unit 2817